Bluetooth Low Energy

RF PHY IP

Description

Celfras BLE RF PHY IP provides a high performance, low power, low cost Bluetooth Low Energy (BLE) radio transceiver solution. The BLE 4.2 compliant IP is tested, qualified, and listed as Declaration ID D036386 (QDID 99277) by Bluetooth SIG.

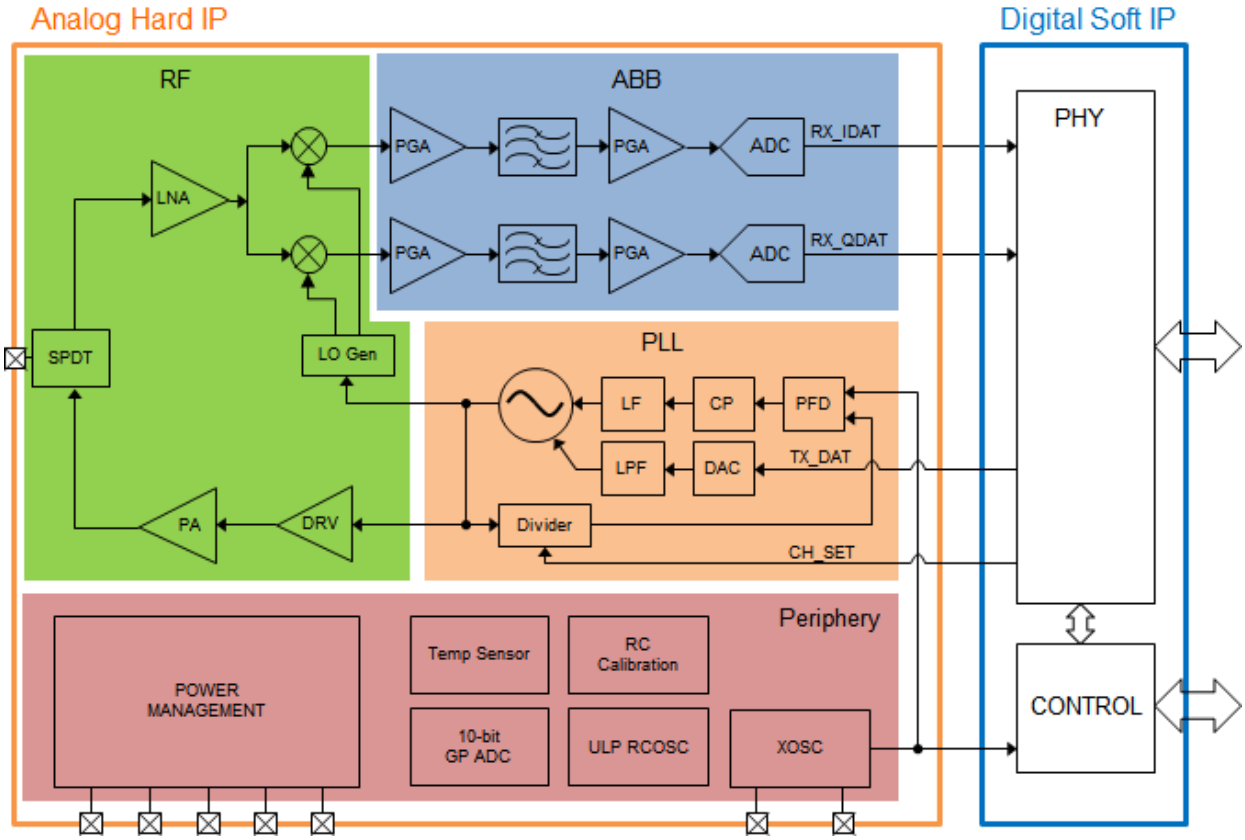
Features

- **Radio**
  - 2.4-GHz CMOS RF transceiver compliant with BLE 4.2 standard
  - Single-ended RF interface with an integrated Rx/Tx switch
  - Excellent receiver sensitivity, selectivity, and blocking performance
  - Programmable output power up to +9dBm in high power mode and up to +0dBm in low power mode
- **Power Management**
  - Integrated switched-capacitor DC-DC converter to eliminate a power inductor
  - Integrated low-noise low drop out regulator
  - Integrated micro-power low drop regulator for always-on blocks
- **Peripherals**
  - 32MHz crystal oscillator with on-chip load capacitors
  - Ultra low power, calibrated 32kHz RC oscillator to eliminate a quartz crystal
  - 10-bit general-purpose SAR ADC
  - Built-in temperature sensor and RC calibration circuit for automatic tuning
- **Digital**
  - 1Mb/s GFSK PHY and controller
- **Current consumption**
  - Active mode Rx : 8 mA@0.9V
  - Active mode Tx (low-power mode) : 10mA@0.9V
  - Sleep mode : 1 uA@Vbat
- **Process node**
  - TSMC 55nm ULP

Deliverables

- **Datasheet**
- **GDSII layout file**
- **Encrypted RTL code**

Block Diagram



Electrical Characteristics

Parameters	Comments	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply voltage	VDD_PA, VDD_IO, DCDC_IN	2.0		3.63	V
	VDD_ABB, VDD_DIG, VDD_AON, VDD_MM, VDD_PLL, VDD_VCO, VDD_RF	0.81	0.9	1.32	V
Temperature	Ambient temperature	-30		85	℃
Receiver					
Sensitivity	PER=30.8%, Dirty Tx disabled (Note 1)		-90		dBm
Max input level	PER=30.8%		0		dBm
Co-channel interferer ratio	Wanted signal at -67dBm@f0 with modulated interferer at f0, PER=30.8%		13		dB
Adjacent (±1MHz) interferer ratio	Wanted signal at -67dBm@f0 with modulated interferer at f0+1MHz/f0-1MHz, PER=30.8%		-4/-4		dB
Adjacent (±2MHz) interferer ratio	Wanted signal at -67dBm@f0 with modulated interferer at f0+2MHz/f0-2MHz, PER=30.8%		-22/-23		dB
Adjacent (±3MHz) interferer ratio	Wanted signal at -67dBm@f0 with modulated interferer at f0+3MHz/f0-3MHz, PER=30.8%		-33/-29		dB
Image frequency interferer ratio	Wanted signal at -67dBm@f0 with modulated interferer at image frequency, PER=30.8%		-19		dB
Adjacent (±1MHz) to Image frequency interferer ratio	Wanted signal at -67dBm@f0 with modulated interferer at image±1MHz, PER=30.8%		-29/-33		dB
Out-of-band blocking	30 MHz – 2000 MHz		-5		dBm
	2003 MHz – 2399 MHz		-15		dBm
	2484 MHz – 2997 MHz		-15		dBm
	3000 MHz – 12.75 GHz		-5		dBm
Intermodulation	Wanted signal at -64dBm@f0 with a sine wave at f1 and modulated interferer at f2, f0=2*f1-f2, |f2-f1|=n*1MHz, n=3,4,5, PER=30.8%		-32		dBm
Gain control range			90		dB
Gain control step size			1		dB
Current consumption	Measured at LDO input			8	mA
Transmitter					
Output power range	Low power mode	-23		1	dBm
	High power mode	-15		9	dBm
Output power in 2nd harmonic	Fundamental signal at 0dBm with low power mode		-50		dBm
Output power in 3rd harmonic	Fundamental signal at 0dBm with low power mode		-55		dBm
Current consumption	Low power mode, measured at LDO input			10	mA

Parameters	Comments	Min	Typ	Max	Unit
Frequency synthesizer					
Reference clock			32		MHz
Rx settling time			TBM		μs
Tx settling time			TBM		μs
DC-DC converter					
Supply voltage	DCDC_IN	2.0		3.63	V
Load current	Active mode		10	20	mA
Switching frequency		0.25		2	MHz
Voltage dropout	10mA load current		100		mV
Flying capacitor			1		μF
Output capacitor			3.3		μF
Startup time	No load, deep-sleep to light-sleep		TBM		μs
LDO regulator					
Supply voltage	DCDC_IN	2.0		3.63	V
Input voltage	DCDC_OUT	1.0		1.8	V
Output voltage	LDO_OUT		0.9		V
Load current			10		mA
Quiescent current	With bandgap reference	22		35	μA
Output capacitor			1		μF
Micro LDO regulator					
Supply voltage	DCDC_IN	2.0		3.63	V
Output voltage	VDD_AON		0.9		V
Load current			1		μA
Quiescent current	With bandgap reference and power-on reset		850		nA
Output capacitor			200		nF
Crystal oscillator					
Oscillator frequency			32		MHz
Crystal parameters	Series resistance			100	Ω
	Load capacitance		8		pF
	Drive level		10	100	μW
	Frequency tolerance at room temp	-10		10	ppm

Parameters	Comments	Min	Typ	Max	Unit
	Frequency characteristics over temperature	-20		20	ppm
Settling time			TBM		ms
ULP RC oscillator					
Oscillator frequency		23	32	46	kHz
Tuning step	Without ΣΔ modulation		0.15		%
	With ΣΔ modulation		0.02		%
Temperature accuracy			0.02		%/℃
Voltage accuracy			0.4		%/V
Quiescent current			250		nA
General purpose ADC					
Resolution			10		bits
Conversion rate		0.5		4	MS/s
Full-scale input	With internal attenuator enabled	0		3.63	V
	With internal attenuator disabled	0		0.9	V
INL			TBM		LSB
DNL			TBM		LSB
ENOB			9		bits

Note 1 : The target receiver sensitivity of -94dBm will be silicon-proven in our revised IP.

Revision History

Date	Version No.	Description
2017/08/25	1.0	Preliminary Release

Contact US

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